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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/588,770

05/09/2007

Yoshihiro Miyake

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7590

01/28/2009

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EXAMINER

STEVENS, THOMAS H

ART UNIT

PAPER NUMBER

2121

MAIL DATE

DELIVERY MODE

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PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/588,770	<b>Applicant(s)</b> MIYAKE, YOSHIHIRO	
	<b>Examiner</b> THOMAS H. STEVENS	<b>Art Unit</b> 2121	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 12/02/2008.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1,3,4,6,7,9,10,12- 14 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,3,4,6,7,9,10,12-14 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)            | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | Paper No(s)/Mail Date. _____                                      |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>08/29/2008</u>  | 6) <input type="checkbox"/> Other: _____                          |

**DETAILED ACTION**

1. Claims 1,3-4,6,7,9,10,13 and 14 were examined.
2. Claims 2,5,8,11 were cancelled.

***Section I: Non-Final Rejection***

***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1,3-4,6,7,9,10, 12- 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Vigoda et al. (US Patent 7,209,867;hereafter Vigoda). Vigoda discloses a signal application process (abstract).

Claim 1: A nonlinear (pg.2, right column, "Vigoda, 'A Nonlinear Dynamic System for Spread Spectrum Code Acquisition') controller (a phase lock loop represents a control event, column 2, line 9) comprising: a first module (e.g., phase comparator of the phase lock loop (well known within the art), column 2, line 1) composed of a nonlinear (pg.2, right column, "Vigoda, 'A Nonlinear Dynamic System for Spread Spectrum Code

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Acquisition') system for creating a synchronous state (suggestion of synchronization, column 2, line 10) with a controlled object through a nonlinear (pg.2, right column, "Vigoda, 'A Nonlinear Dynamic System for Spread Spectrum Code Acquisition') interaction with the controlled object; and a second module (e.g., low pass filter of the phase lock loop (well known within the art), column 2, line 1) composed of a feedback system (e.g., phase lock loop (well known within the art), column 2, line 1) for adjusting a parameter to vary a relation value of the first module (e.g., phase comparator of the phase lock loop (well known within the art), column 2, line 1) relating to the synchronization with the controlled object based on a difference between the relation value and a target relation value (target is the level of proportion to be the phase difference between the incoming data stream/frequency and the voltage control oscillator of the phase lock loop, column 2, line 9), wherein the controlled object is controlled by convergence of the relation value relating to the synchronization of the first module (e.g., phase comparator of the phase lock loop (well known within the art), column 2, line 1) to the target relation value (target is the level of proportion to be the phase difference between the incoming data stream/frequency and the voltage control oscillator of the phase lock loop, column 2, line 9): and the first module (e.g., phase comparator of the phase lock loop (well known within the art), column 2, line 1) vibrates at different natural frequencies from the controlled object, and the nonlinear (pg.2, right column, "Vigoda, 'A Nonlinear Dynamic System for Spread Spectrum Code Acquisition') interaction has an entrainment effect.

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Claim 3: The nonlinear (pg.2, right column, "Vigoda, 'A Nonlinear Dynamic System for Spread Spectrum Code Acquisition') controller (a phase lock loop represents a control event, column 2, line 9) as recited in Claim 1, wherein the relation value relating to the synchronization is a phase difference between a vibration of the controlled object and a vibration of the first module, and a parameter is the natural frequency of the first module.

Claim 4: The nonlinear (pg.2, right column, "Vigoda, 'A Nonlinear Dynamic System for Spread Spectrum Code Acquisition') controller (a phase lock loop represents a control event, column 2, line 9) as recited in claim 1, wherein the synchronous state (suggestion of synchronization, column 2, line 10) between the first module (e.g., phase comparator of the phase lock loop (well known within the art), column 2, line 1) and the controlled object is achieved through transmission and reception of rhythm.

Claim 6: The nonlinear (pg.2, right column, "Vigoda, 'A Nonlinear Dynamic System for Spread Spectrum Code Acquisition') controller (a phase lock loop represents a control event, column 2, line 9) as recited in Claim 3, wherein the synchronous state (suggestion of synchronization, column 2, line 10) between the first module (e.g., phase comparator of the phase lock loop (well known within the art), column 2, line 1) and the controlled object is achieved through transmission and reception of rhythm.

Claim 7: The nonlinear (pg.2, right column, "Vigoda, 'A Nonlinear Dynamic System for Spread Spectrum Code Acquisition') controller (a phase lock loop represents a control

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event, column 2, line 9) as recited in Claims 1, wherein the synchronous state (suggestion of synchronization, column 2, line 10) between the first module (e.g., phase comparator of the phase lock loop (well known within the art), column 2, line 1) and the controlled object is achieved through a radio wave (adjusting the input frequency or data stream of the phase lock loop, column 2, line 2-6) or network.

Claim 9: The nonlinear (pg.2, right column, "Vigoda, 'A Nonlinear Dynamic System for Spread Spectrum Code Acquisition') controller (a phase lock loop represents a control event, column 2, line 9) as recited in Claim 3, wherein the synchronous state (suggestion of synchronization, column 2, line 10) between the first module (e.g., phase comparator of the phase lock loop (well known within the art), column 2, line 1) and the controlled object is achieved through a radio wave (adjusting the input frequency or data stream of the phase lock loop, column 2, line 2-6) or network.

Claim 10: The nonlinear (pg.2, right column, "Vigoda, 'A Nonlinear Dynamic System for Spread Spectrum Code Acquisition') controller (a phase lock loop represents a control event, column 2, line 9) as recited in Claim 4, wherein the synchronous state (suggestion of synchronization, column 2, line 10) between the first module (e.g., phase comparator of the phase lock loop (well known within the art), column 2, line 1) and the controlled object is achieved through a radio wave (adjusting the input frequency or data stream of the phase lock loop, column 2, line 2-6) or network.

Claim 12: The nonlinear (pg.2, right column, "Vigoda, 'A Nonlinear Dynamic System for Spread Spectrum Code Acquisition') controller (a phase lock loop represents a control

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event, column 2, line 9) as recited in Claim 6, wherein the synchronous state (suggestion of synchronization, column 2, line 10) between the first module (e.g., phase comparator of the phase lock loop (well known within the art), column 2, line 1) and the controlled object is achieved through a radio wave (adjusting the input frequency or data stream of the phase lock loop, column 2, line 2-6) or network.

Claim 13: A nonlinear (pg.2, right column, "Vigoda, 'A Nonlinear Dynamic System for Spread Spectrum Code Acquisition') control method comprising: creating a synchronous state (suggestion of synchronization, column 2, line 10) with a controlled object through a nonlinear (pg.2, right column, "Vigoda, 'A Nonlinear Dynamic System for Spread Spectrum Code Acquisition') interaction with the controlled object; acquiring a state variable (represents part of the control analysis of the phase lock loop program, column 2, line 9) relating to a dynamic behavior of the controlled object; adjusting a parameter for varying a relation value relating to the synchronization with the controlled object based on a difference between the relation value relating to the synchronization and a target relation value (target is the level of proportion to be the phase difference between the incoming data stream/frequency and the voltage control oscillator of the phase lock loop, column 2, line 9); and creating a new synchronous state (suggestion of synchronization, column 2, line 10) with the controlled object using the adjusted parameter (adjusting the input frequency or data stream of the phase lock loop, column 2, line 2-6).

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Claim 14: A program readable by a controller (a phase lock loop represents a control event, column 2, line 9) for causing the controller (a phase lock loop represents a control event, column 2, line 9) to perform the nonlinear (pg.2, right column, "Vigoda, 'A Nonlinear Dynamic System for Spread Spectrum Code Acquisition') control method as recited in Claim 13.

## ***Section II: Response to Arguments***

### ***Incorporation by Reference***

5. It appears applicants have not responded to this issue, thus objection is maintained.

**112 2<sup>nd</sup>**

6. Withdrawn.

### ***Conclusion***

7. The prior art made of record and not relied upon is considered pertinent to applicants' disclosure:

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- Miller G.M., "Modern Electronic Communication" 1998 pg. 209 and 209: discloses the particulars of a phase lock loop circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mr. Tom Stevens whose telephone number is 571-272-3715.

If attempts to reach the examiner by telephone are unsuccessful, please contact examiner's supervisor Mr. Albert Decady (571-272-3819). The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Answers to questions regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) (toll-free (866-217-9197)).

/Thomas H. Stevens/

Examiner, Art Unit 2121

/Albert Decady /  
Supervisory Patent Examiner  
Tech Center 2100

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